Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 7. A bump layout on a driver integrated circuit (IC), comprising:
a narrow and long driver IC package having an active region, wherein the package has a first short side, a second short side, a first long side and a second long side; and
a plurality of bumps over the active region close to the first long side and the second long side and over some other part of the active region so that the active region is divided into a plurality of circuit blocks.

[c2] 9. The bump layout of claim 7, wherein the bumps close to the first long side are positioned in a vertically aligned grid format.

[c3] 10. The bump layout of claim 7, wherein the bumps close to the first long side are positioned in alternatively staggered row format.

[c4] 11. The bump layout of claim 7, wherein the bumps close to the second long side are positioned in a vertically aligned grid format.

[c5] 12. The bump layout of claim 7, wherein the bumps close to the second long side are positioned in an alternatively staggered row format.

[c6] 13. The bump layout of claim 7, wherein the circuit blocks are electrically connected by circuit lines.